ABSTRACT OF THE DISCLOSURE

The switching between the normal operation mode and the memory operation mode is achieved by disposing one retaining circuit 110 for a plurality of pixel elements (for example, 2 or 4 pixel elements). The retaining circuit 110, which is a SRAM, requires considerable circuit space. The sharing of one retaining circuit by a plurality of the pixel elements enables the reduction of the seeming "number of the pixel elements" under the memory operation mode. This can lead to the size reduction of the pixel element, achieving the finer display under the normal operation mode. Also, the reduction in the number of the retaining circuits can further reduce the energy consumption under the memory operation mode, comparing to the case where the retaining circuit 110 is disposed for each of the pixel elements.